Claims

- 1 1. A signal amplifier comprising:
- 2 at least two capacitive elements configured to retain a charge;
- an interconnection of active devices between the at least two capacitive elements
- 4 configured to operate upon a transient charge flow as a current when in operation,
- 5 wherein the charge flow is partitioned into at least two parts according to a controlling
- 6 parameter.
- 1 2. A signal amplifier according to Claim 1 wherein the at least two active elements are three terminal devices.
- 1 3. A signal amplifier according to Claim 1 wherein the at least two active
- 2 elements are three terminal devices configured as long tailed pairs, each having a
- 3 commonly connected terminal, wherein the transient charge flow enters the commonly
- 4 connected terminals, and the signal amplifier further comprising a partition defined by
- 5 the total charge sent to each output terminal and the controlling parameter is the input
- 6 voltage difference.
- 4. A signal amplifier according to Claim 3, wherein the three terminal
- 2 devices are MOSFET devices, wherein the commonly connected terminals are the source
- 3 terminals of the devices, wherein the partition is the total charge sent to the separate drain
- 4 terminals and wherein the controlling parameter is the voltage difference between the
- 5 gate connections.
- 1 5. A signal amplifier according to Claim 3 further comprising a first
- 2 capacitor and at least two secondary capacitors, wherein the long tailed pair is configured
- 3 to partition a charge that transiently flows between the first capacitor and the two
- 4 secondary capacitors such that, upon cessation of the transient current, an output voltage
- 5 difference is expressed between the two secondary capacitors that is a representation of
- 6 the input voltage between the two gate connections.

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1	6. A signal amplifier according to Claim 3 wherein the output voltage is an	
2	amplified version of the input voltage.	
1	7. A current mode switched capacitor comprising:	
2	a long tailed pair of transistors, each having one terminal connected to a commo	n
3	voltage source and each connected in common by another terminal;	
4	a cascode device connected at one terminal to the connected terminals of the lon	g
5	tailed pair;	
6	a switched capacitor circuit connected on one end to another terminal of the	
7	cascode device and at another end to ground, and where the gate of the cascode device i	.S
8	connected to a bias voltage source, the switched capacitor circuit having a capacitor	
9	connected at one terminal to the source of the cascode device, and a switch connected a	t
10	one terminal to the cascode device, another terminal connected to one end of a grounded	d
11	current source, and yet another terminal connected to the common voltage source.	
1	8. A method of amplifying a signal, comprising:	
2	receiving an input signal;	
3	opening a switch to cause the current from a current source to flow through the	
4	long tailed pair via the cascode device until the voltage in the capacitor drops;	
5	cutting off the current source in response to the voltage in the capacitor dropping	g;
6	and	
7	closing the switch to cause the capacitor to charge up to the reference voltage.	
1	9. A circuit, comprising:	
2	a load circuit configured to generate a load current in response to an input signal	ί;
3	an improved switched capacitor circuit configured to, wherein the switched	
4	capacitor includes a connection charge transferring circuit configured to utilize the char	ge
5	transiently entering or leaving the switched capacitor circuit as an output parameter,	
6	retain this charge after a charge transfer, wherein the partitioning of the charge may hav	e

depended on an auxiliary input parameter.

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- 1 10. A circuit according to Claim 3, further comprising a long tailed pair,
- wherein the auxiliary input parameter is the difference in input gate voltages.
- 1 11. A circuit comprising:
- a long tailed pair input circuit configured to operate over a finite time interval
- 3 over which a specified current flows such that a prescribed finite charge has passed at the
- 4 end of this time interval, the circuit being configured to assess the total charge that has
- 5 been partitioned as an output parameter during a finite time interval.